26.6 A 0.05×0.05mm² RFID Chip with Easily Scaled-Down ID-Memory

Mitsuo Usami[1], Hisao Tanabe[1], Akira Sato[1], Isao Sakama[1], Yukio Maki[2], Toshiaki Iwamatsu[2], Takashi Ipposhi[2], Yasuo Inoue[2]

[1]Hitachi, Tokyo, Japan
[2]Renesas Technology, Hyogo, Japan

This paper describes an ultra-small radio frequency identification (RFID) [1] chip using electron beam (EB) writing for forming easily scaled-down ID-memory. Recently, RFID devices have been recognized as being useful ID carriers for accessing Internet databases, by having a unique Internet protocol (IP) address. Therefore, memory technology has become the most important consideration when developing new RFID chips. Moreover, ultra-thin and ultra-small chips are indispensable because they are cheaper and more reliable than conventional chips. Silicon-on-insulator (SOI) 90nm CMOS process and double-surface electrode chip structures enable the design of 0.05×0.05mm² and 5μm-thick RFID chips with small, low-cost and highly-reliable ID-memory employing 128b EB-written technology.

We develop an ultra-small RFID chip. Figure 26.6.1 shows the circuit structure of the chip. A 128-bit EB-written memory is controlled by a binary counter consisting of a separate 3b control counter for the memory control and, 4b and 3b memory address counters. Each counter is connected in series. There is no need for peripheral circuits to write ID-data to the memory, which helps reduce chip size. The memory control circuit drives the memory cell, which is selected by the X- and Y-decoders depending on the contents of the 3b control counter. Each bit of the memory controls the impedance of the power rectifier circuit. The front-end circuits of this chip are constructed as conventional clock envelopment circuits and conventional power rectifier circuits, which are attached to an antenna. Each diode is made by active body contact SOI NMOS transistors to reduce the forward-bias voltage [2]. Furthermore, diodes are arranged in arrays of transistors with restricted channel widths to reduce the body resistance of the SOI transistors,

Figure 26.6.2 shows circuit details of the 128b EB-written memory. Each memory cell consists of one transistor, which has an EB programming connection terminal. The connection information is detected by a simple precharge and discharge circuit mechanism. All the drains of the NMOS transistors in the memory cell are commonly connected and store precharge electrons through a PMOS transistor, which is controlled by the memory control circuit. EB programming is performed by open or short connection conditions between each NMOS transistor's source and a common line that is connected to a Y-decoder selection transistor.

This EB-written memory structure has several advantages over other memory technologies. First of all, it is adaptable for use in small RFID devices that use finer device processes because the memory circuit consists of ultra-small transistors and requires no high-voltage endurance to write to memory cells. Second, the reliability of RFIDs under various circumstances, such as when exposed to severe temperatures (i.e., 400°C), mechanical stress or radiation, is excellent. Third, maintaining highly secure manufacturing and efficiently controlling the issuing of ID numbers to keep numbering unique during high-volume production is possible because batch EB writing of ID numbers is done during the wafer fabrication process. Finally, EB technology can generate unique ID patterns without using expensive one-time-use glass masks.

When using EB writing to ultra-small RFID chips, it is necessary to consider the fabrication throughput. Figure 26.6.3 shows chip-grouped EB writing. Chip-grouped EB writing drastically increases fabrication efficiency. The chip-group size can be up to 10,000 chips per one EB shot. EB write-time is reduced using volume group writing 50× compared with individual writing. The ID number of each chip is controlled by highly secure server systems. ID number patterns are merged with the peripheral circuit patterns of the RFID chip and transferred to the EB equipment. Then, group EB writing directly to each chip is done as if the writing was being done to a single large chip.

It is indispensable to have double-surface electrodes for ultra-small chips [3,4], Figure 26.6.4 is a cross section showing a conduction pin structure penetrating a buried oxide (Box) layer. Conduction pins are easily formed when active devices are formed on an SOI wafer. After removing the substrate of Si, Au is sputtered onto the Box to make a back electrode, which enables a connection to be made to the circuit devices through this conduction pin. The impedance of the back electrode is reduced by designing multiple conduction pins. The Au top electrode is formed on an Al pad, which is used for wafer proving of dedicated design testchips distributed on the wafer. The final thickness of a double-surface chip is only 5μm. RF and memory circuits are interconnected by two-layer copper metallization. The minimum gate length of a transistor is 90nm. Trench isolation of the SOI has two levels: full and half. The half-trench isolation is useful for making active body contact. Each ultra-thin chip on the wafer is separated by dry etching with a narrow separation gap between chips, which increases ultra-small chip fabrication numbers per wafer. Another advantage of dry etching separation is that it reduces chipping around the chip, which means semiconductor chips are inserted more easily into paper material, increasing the mechanical strength for many paper applications.

Figure 26.6.5 shows the normal operation of this chip by displaying waveforms on an RFID reader. The carrier frequency is 2.45GHz. The 100kHz full-ASK clock signals are modulated. The reader detects ID-data from this ultra-small chip by monitoring reflection levels from the chip. The reader verifies the ID-data by calculating an error-check code on the detected ID-data. The maximum communication range is measured to be 300mm, even though it is an ultra-small chip.

Figure 26.6.6 shows a micrograph of the chip. The chip size is 0.05×0.05mm². To show the chip in detail, the upper aluminum metal is removed. The 128b ID-memory size is 21×31μm², including the control counter, address counters and decoders. This ultra-small and ultra-thin RFID chip enables the opening of a new application market.

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References:
[1] D. Friedman, H. Heinrich, and D.-W. Duan, "A Low-Power CMOS Integrated Circuit for Field-Powered Radio Frequency Identification Tags," *ISSCC Dig. Tech. Papers*, pp. 294-295, Feb. 1997.
[2] Y. Hirano, T. Matsumoto, S. Maeda, et al., "Impact of 0.10-μm SOI CMOS with Body-Tied Hybrid Trench Isolation Structure to Break Through the Scaling Crisis of Silicon Technology," *IEDM Tech. Dig.*, pp. 467-470, Dec., 2000.
[3] S. Briole, C. Pacha, K. Goser, et al., "AC-Only RF ID Tags for Barcode Replacement," *ISSCC Dig. Tech. Papers,* pp. 438-439, Feb., 2004.
[4] M. Usami, A. Sato, H. Tanabe, et al., "An SOI-Based 7.5μm-Thick 0.15 x 0.15mm² RFID Chip," *ISSCC Dig. Tech. Papers*, pp. 308-309, Feb., 2006.

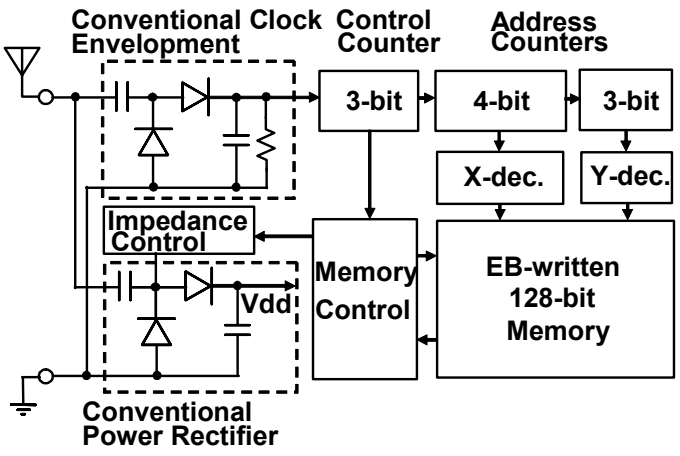

Figure 26.6.1: Circuit structure of ultra-small RFID chip.

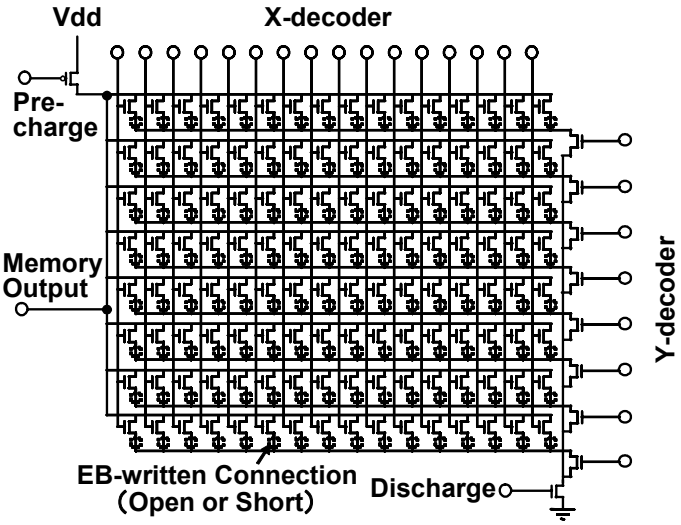

Figure 26.6.2: EB-written 1T memory cells for RFID chip.

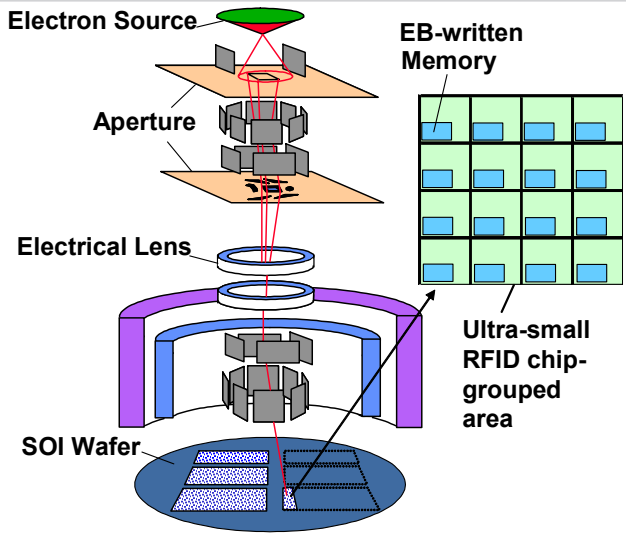

Figure 26.6.3: Chip-grouped EB writing to increase fabrication efficiency of ultra-small RFID chips.

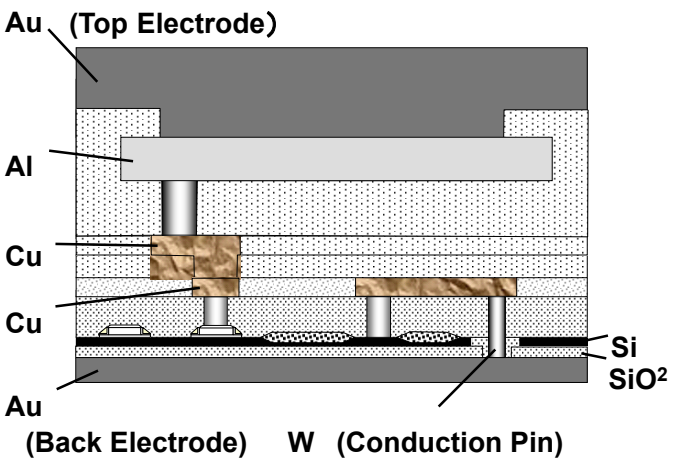

Figure 26.6.4: Conductive pin to back electrode of SOI RFID chip to realize double-surface electrode structure (cross section).

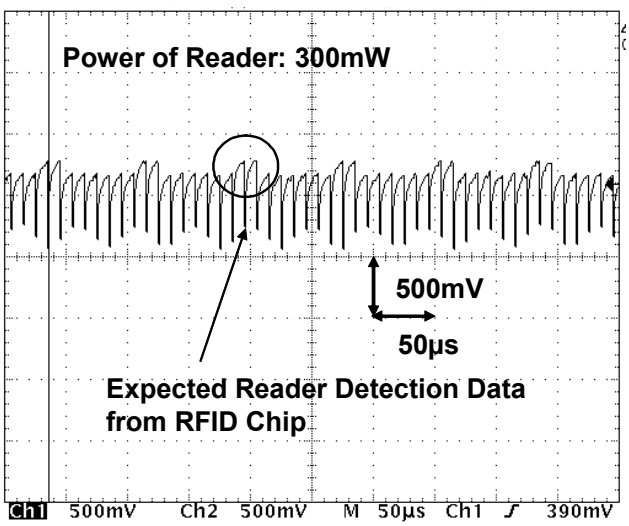

Figure 26.6.5: Reader detection signal of normal ID number from ultra-small RFID chip.

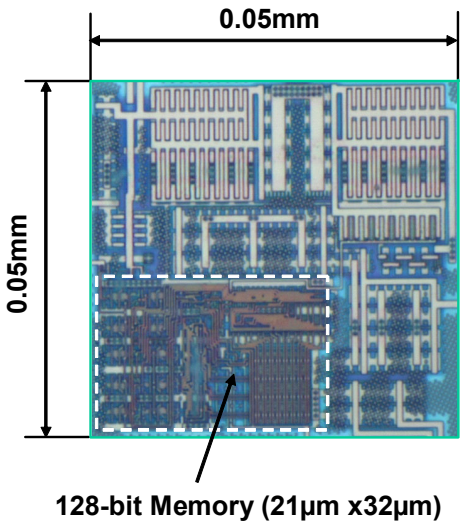

Figure 26.6.6: Micrograph of ultra-small RFID chip.